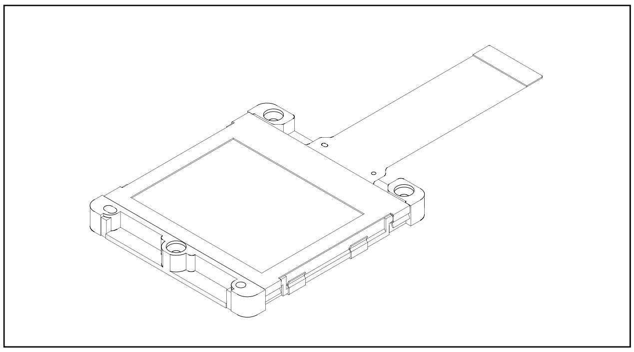
SONY

LCX036AMT

4.6cm (1.8-type) Black-and-White LCD Panel

Description



The LCX036AMT is a 4.6cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX036AMT panels provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of a dot-line inverse driving system, 2-series gate pulse driving systems, dot-sequential + lump precharge driving system and a gate wsi structure realizes high picture quality and a high aperture ratio.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

Features

- Number of active dots: 1,931,216 (1.8-type, 4.6cm in diagonal)
- High optical transmittance: 25% (typ.)
- Built-in dot-line inverse driving circuit
- Built-in 2-series gate pulse driving circuits
- Built-in dot-sequential + collective precharge driving circuit
- High contrast ratio with normally white mode: 400 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function
- Antidust glass package
- Microlens used

Element Structure

- Dots: 1604 (H) × 1204 (V) = 1,931,216
- Active matrix panel with built-in peripheral driver using polycrystalline silicon super thin film transistors

Applications

- Liquid crystal data projectors
- Liquid crystal multimedia projectors
- Liquid crystal rear-projector TVs, etc.

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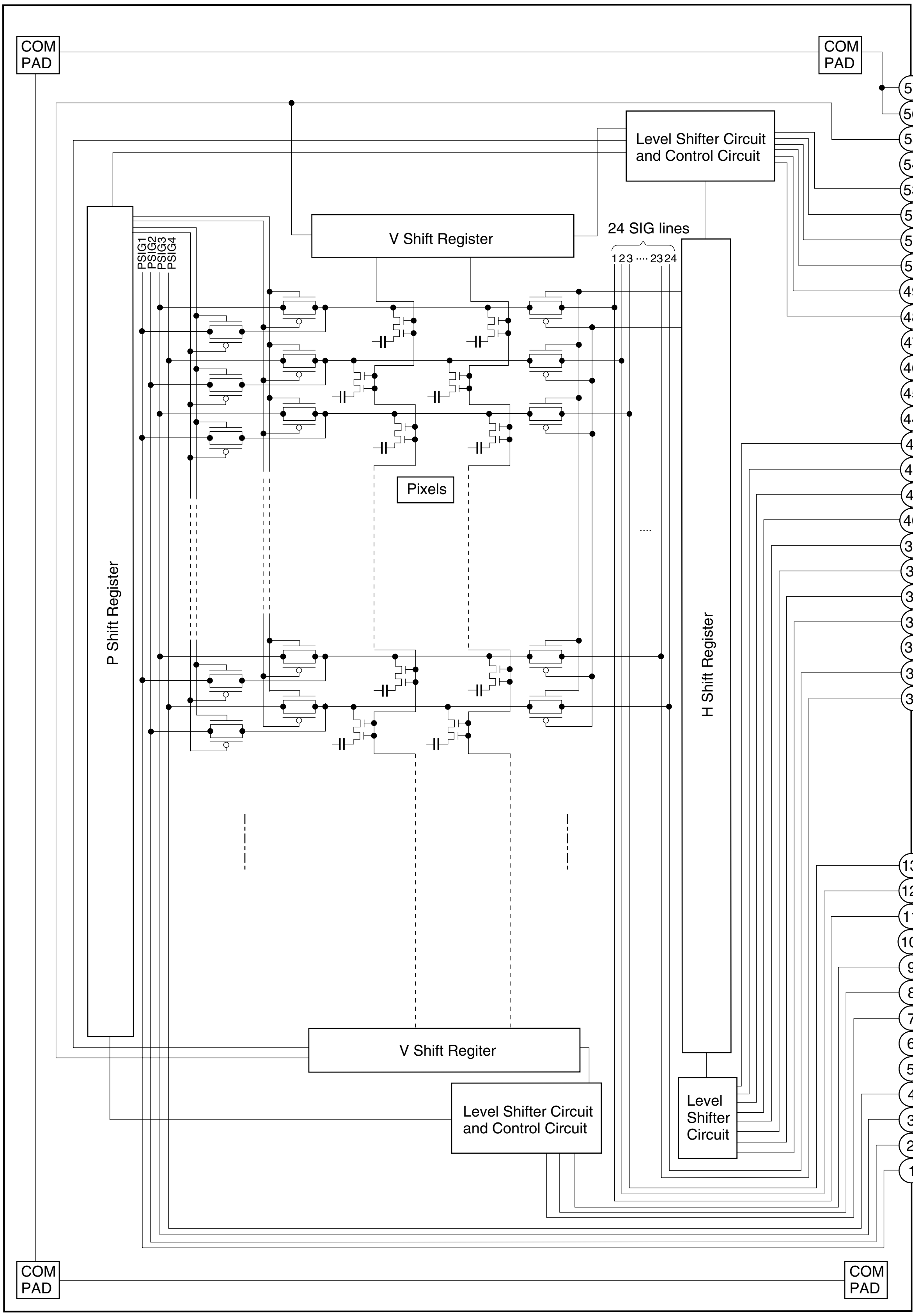
E00Z03A15

Block Diagram

The block diagram is shown below.



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• P driver supply voltage	PV_{DD}	–1.0 to +20	V
• V driver supply voltage	$VV_{DD}L$, $VV_{DD}R$, $VV_{DD}H$	–1.0 to +20	V
• Common pad voltage	VCOM	–1.0 to +17	V
• H shift register input pin voltage	HST, RGT, HCK, HCKX, DCK1, DCK1X, DCK2, DCK2X	–1.0 to +17	V
• P shift register input pin voltage	PST, PCG	–1.0 to +17	V
• V shift register input pin voltage	VST, VCKL, VCKR, DWN, ENBL, ENBR	–1.0 to +17	V
• Video signal input pin voltage	VSIG1 to 24, PSIG1 to 4	–1.0 to +15	V
• Operating temperature*	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

* LCD panel temperature inside the antidust glass

Operating Conditions (V_{SS} = 0V)

• Supply voltage

HV_{DD}	15.5 ± 0.5V
PV_{DD}	15.5 ± 0.5V
$VV_{DD}R$	15.5 ± 0.5V
$VV_{DD}L$	15.5 ± 0.5V
$VV_{DD}H$	15.5 ± 0.5V

• Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

Vin	5.0 ± 0.5V

Pin Description

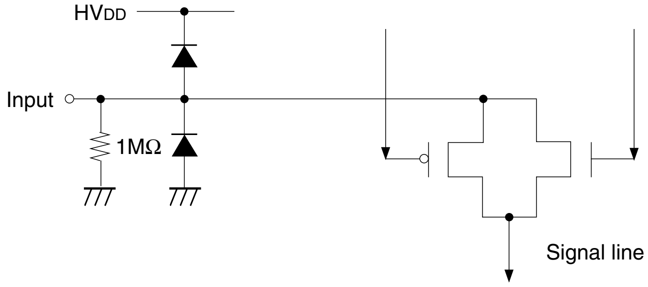
Pin No.	Symbol	Description
1	PSIG1	Uniformity improvement signal input (for black)
2	PSIG2	Uniformity improvement signal input (for black)
3	PSIG3	Uniformity improvement signal input (for gray)
4	PSIG4	Uniformity improvement signal input (for gray)
5	$V_{SS}R$	GND for right V scanner
6	$V_{SS}R$	GND for right V scanner
7	PCG	Uniformity improvement pulse input
8	VCKR	Clock input for right V scanner
9	ENBR	Enable input for right V scanner
10	$VV_{DD}R$	Power supply input for right V scanner
11	VSIG1	Video signal 1 input to panel
12	VSIG2	Video signal 2 input to panel
13	VSIG3	Video signal 3 input to panel
14	VSIG4	Video signal 4 input to panel
15	VSIG5	Video signal 5 input to panel
16	VSIG6	Video signal 6 input to panel
17	VSIG7	Video signal 7 input to panel
18	VSIG8	Video signal 8 input to panel
19	VSIG9	Video signal 9 input to panel
20	VSIG10	Video signal 10 input to panel
21	VSIG11	Video signal 11 input to panel
22	VSIG12	Video signal 12 input to panel
23	VSIG13	Video signal 13 input to panel
24	VSIG14	Video signal 14 input to panel
25	VSIG15	Video signal 15 input to panel
26	VSIG16	Video signal 16 input to panel
27	VSIG17	Video signal 17 input to panel
28	VSIG18	Video signal 18 input to panel
29	VSIG19	Video signal 19 input to panel
30	VSIG20	Video signal 20 input to panel
31	VSIG21	Video signal 21 input to panel
32	VSIG22	Video signal 22 input to panel
33	VSIG23	Video signal 23 input to panel
34	VSIG24	Video signal 24 input to panel

Pin No.	Symbol	Description
35	HV_{DD}	Power supply input for H driver
36	DCK2	Uniformity improvement clock input 1
37	DCK2X	Uniformity improvement clock input 2
38	DCK1X	Uniformity improvement clock input 3
39	DCK1	Uniformity improvement clock input 4
40	HCK	Clock input for H shift register drive
41	HCKX	Clock input for H shift register drive
42	RGT	Drive direction input for H shift register (H: normal, L: reverse)
43	HST	Start pulse input for H shift register drive
44	$V_{SS}L$	GND for left V scanner
45	$V_{SS}L$	GND for left V scanner
46	$VV_{DD}H$	Pixel gate voltage input
47	$VV_{DD}L$	Power supply input for left V scanner
48	ENBL	Enable input for left V scanner drive
49	VCKL	Clock input for left V scanner drive
50	VST	Start pulse input for left and right V scanner drive
51	DWN	Drive direction input for left and right V scanner (H: normal, L: reverse)
52	PST	Start pulse input for P shift register drive
53	SOUT	Test. Leave open.
54	PV_{DD}	Power supply input for P scanner
55	$V_{SS}G$	GND for V gate
56	VCOM	Common voltage of panel
57	VCOM	Common voltage of panel

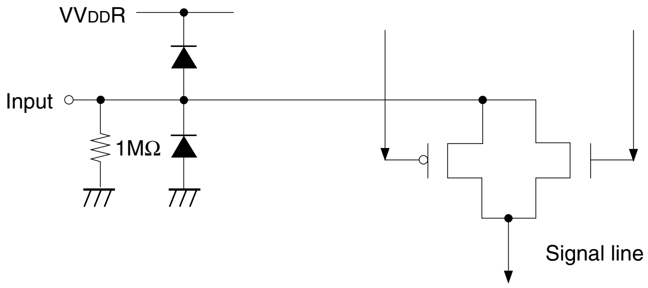
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

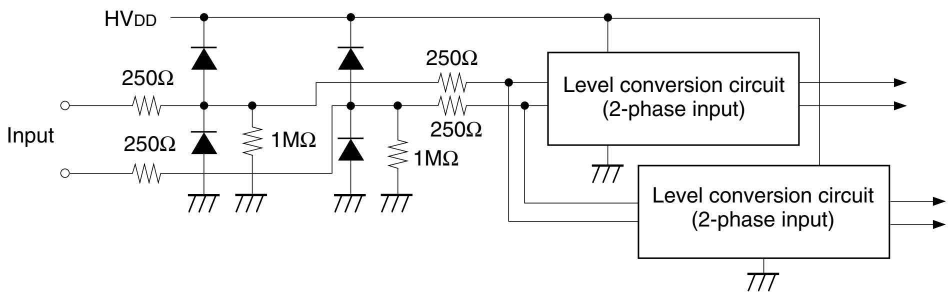
(1) VSIG1 to VSIG24



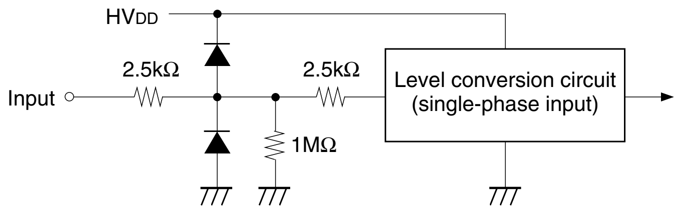
(2) PSIG1 to PSIG4



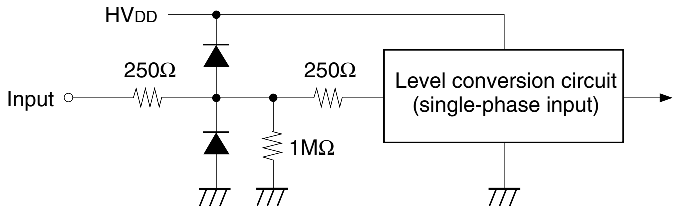
(3) HCK, HCKX, DCK1, DCK1X, DCK2, DCK2X



(4) RGT

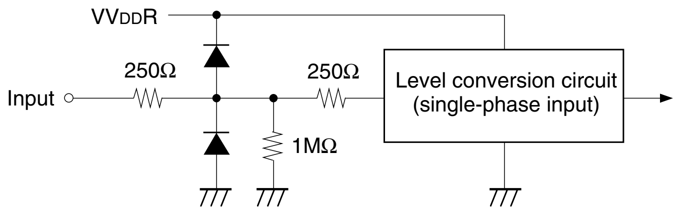


(5) HST

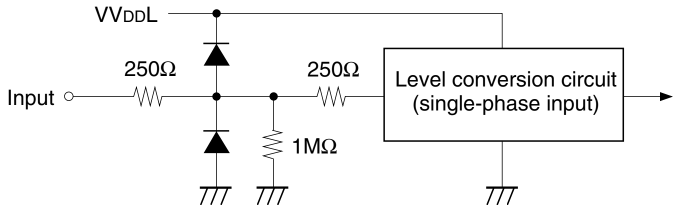


⏚ are all Vss.

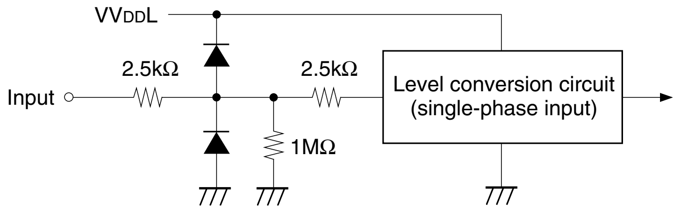
(6) PCG, VCKR



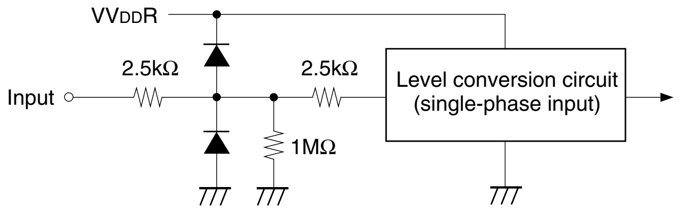
(7) PST, VCKL



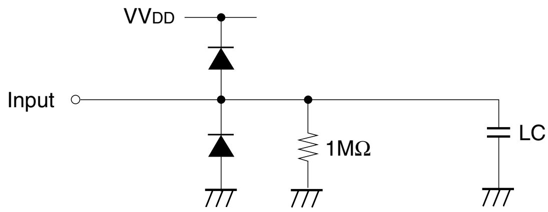
(8) DWN, VST, ENBL, SOUT



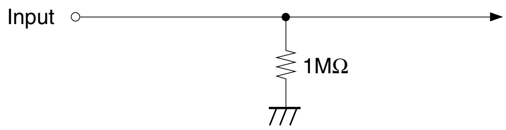
(9) ENBR



(10) VCOM



(11) HV_{DD}, $V_{SS}G$, $VV_{DD}R$, $VV_{DD}L$, $VV_{DD}H$, PV_{DD}



are all V_{SS}.

Input Signals

1. Input signal voltage conditions (Vss = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK, HCKX, DCK1, DCK1X, DCK2, DCK2X	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage VCKL, VCKR, ENBL, ENBR, VST, PCG, DWN	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC	7.4	7.5	7.6	V
Video signal input range*1		Vsig	VVC – 4.5	7.5	VVC + 4.5	V
Common voltage of panel*2		Vcom	VVC – 0.7	VVC – 0.6	VVC – 0.5	V
Uniformity improvement signal input voltage (PSIG)*3		VpsigB	VVC ± 4.4	VVC ± 4.5	VVC ± 4.6	V
		VpsigG	VVC ± 1.7	VVC ± 1.8	VVC ± 1.9	

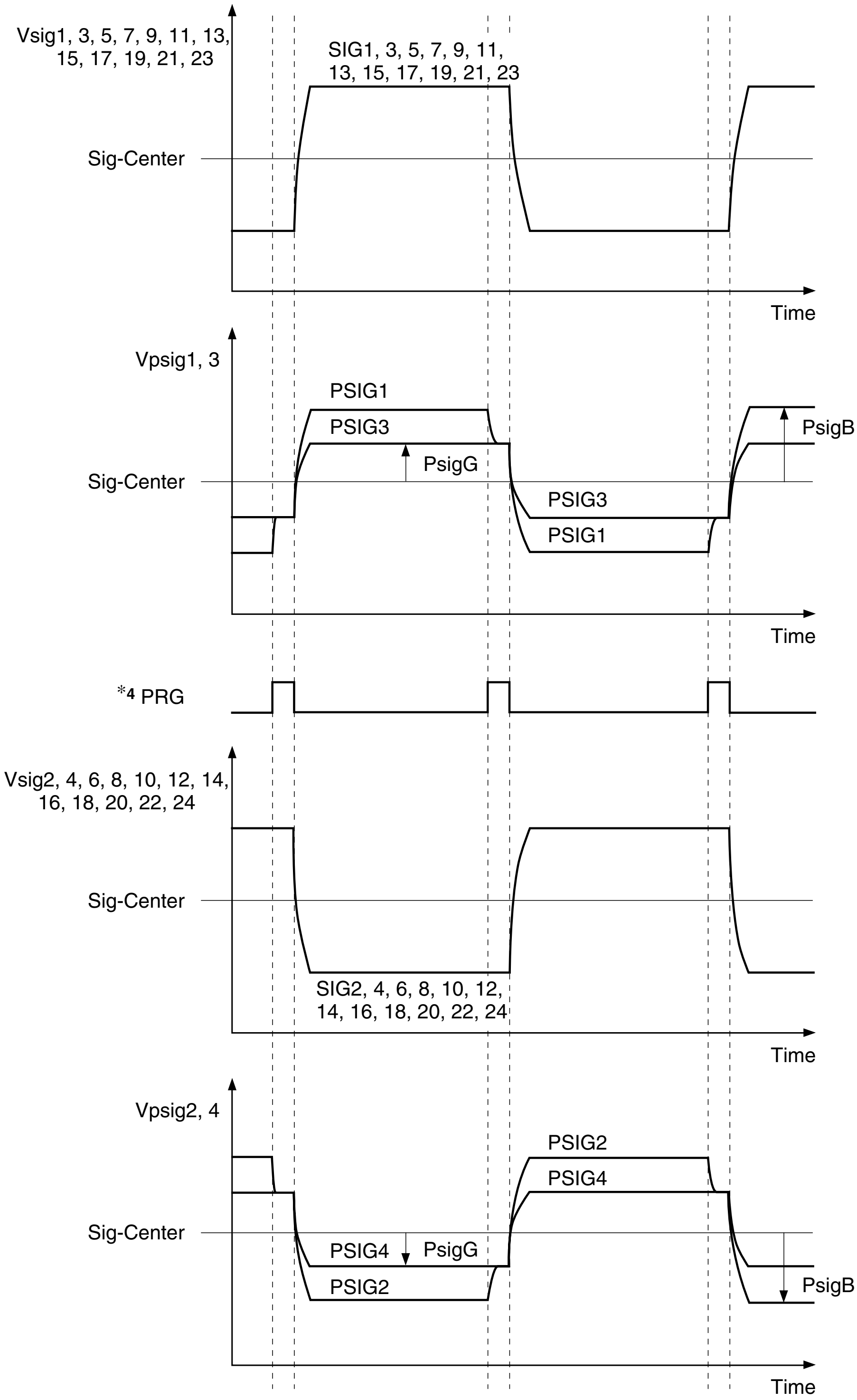
*1 Input video signals shall be symmetrical to VVC.

*2 The typical value of the common pad voltage may lower its suitable voltage according to the set construction used. In this case, use the voltage of which has the maximum contrast as the typical value. When the typical value is lowered, the maximum and minimum values may also lower.

*3 Input the video signals and uniformity improvement signal in the phases shown in the following page.
The PSIG1 and PSIG2 waveforms have 2 steps as shown in the charts on the following page. In the upper chart, the upper value shows the signal level of the first step, and the lower value shows the signal level of the second step.
Here, the rise and fall of PsigB to PsigG in PSIG1 and PSIG2 should be synchronized with the rising edge of the PRG pulse, and the PSIG1 to PSIG4 polarity inversion relative to VCC should be synchronized with the falling edge of the PRG pulse. Also, the PSIG1 to PSIG4 rise time and fall time should be kept within 400ns.

*4 PRG shows the PSIG signal level transition timing, and it is not input to the panel.

Phase Relationship of Video Signal and Uniformity Improvement Signal



LCX036AMT Level Conversion Circuit

The LCX036AMT has a built-in level conversion circuit in the clock input block on the panel. The input signal level increases to HV_{DD}, $VV_{DD}L$, $VV_{DD}R$ or PV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

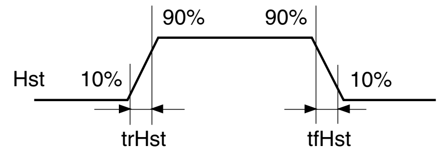
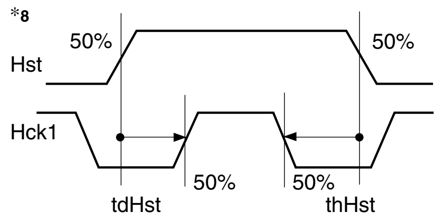
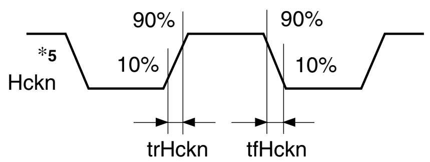
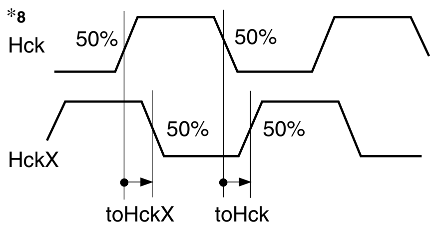
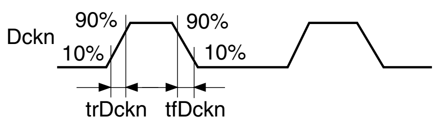
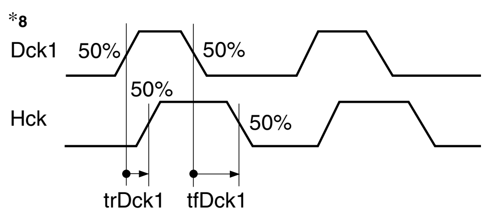
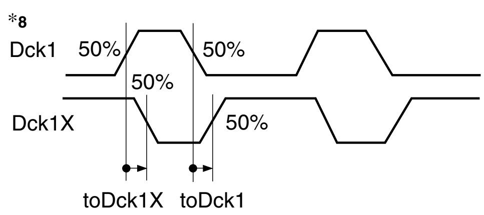
2. Clock timing conditions (Ta = 25°C) (UXGA mode: fHckn = 3.33MHz, fVck = 38.2kHz, fv = 60Hz)

Item		Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data setup time	tdHst	55	65	75	
	Hst data hold time	thHst	55	65	75	
HCK	Hckn rise time*5	trHckn	—	—	30	
	Hckn fall time*5	tfHckn	—	—	30	
	Hck fall to HckX rise time	toHck	–15	0	15	
	Hck rise to HckX fall time	toHckX	–15	0	15	
DCK	Dckn rise time*6	trDckn	—	—	30	
	Dckn fall time*6	tfDckn	—	—	30	
	Dck1 rise to Hck rise time	trDck1	–5	0	5	
	Dck1 fall to Hck fall time	tfDck1	40	50	60	
	Dck1 rise to Dck1X fall time	toDck1X	–5	0	5	
	Dck1 fall to Dck1X rise time	toDck1	–5	0	5	
	Dck2 rise to HckX rise time	trDck2	–5	0	5	
	Dck2 fall to HckX fall time	tfDck2	40	50	60	
	Dck2 rise to Dck2X fall time	toDck2X	–5	0	5	
	Dck2 fall to Dck2X rise time	toDck2	–5	0	5	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data setup time	tdVst	4	6	8	μs
	Vst data hold time	thVst	4	6	8	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Horizontal video period completed to Enb fall time	tdEnb	500*7	600	—	
	Enb fall to Vck rise/fall time	toVck	550	600	650	
	Enb pulse width	twEnb	1200	—	—	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Enb fall to Pcg rise time	toPcg	550	600	650	
	Pcg pulse width	twPcg	300	350		

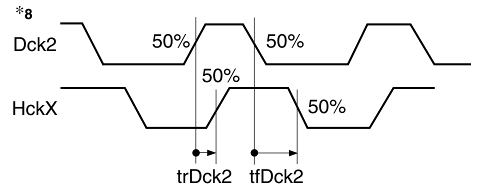
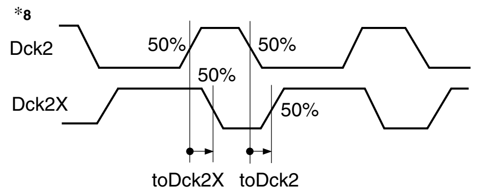
*5 Hckn means Hck and HckX.
*6 Dckn means Dck1, Dck1X, Dck2 and Dck2X.
*7 The minimum value of tdEnb is 500ns. When H-BLK has a long period and has some time to spare, take more time for tdEnb prior to other values.

Item		Symbol	Min.	Typ.	Max.	Unit
PRG	Pcg rise to PRG rise time	tdPRG	200	250	300	ns
	Pcg fall to PRG fall time	thPRG	200	250	300	
	PRG pulse width	twPRG	800	850	900	
PST	Pst rise time	trPst	—	—	30	
	Pst fall time	tfPst	—	—	30	
	Pst data setup time	tdPst	55	65	75	
	Pst data hold time	thPst	55	65	75	
	Enb rise to Pst rise time	toPst	300	350	400	
	Pst rise to Hst rise time	toHst	—	2.5	—	2.5 HCK cycles

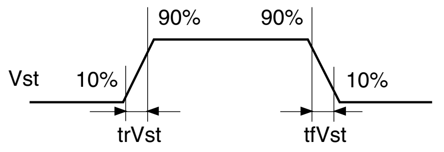
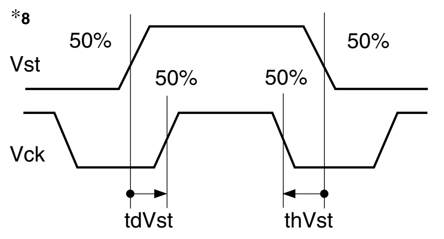
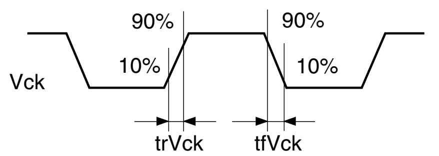
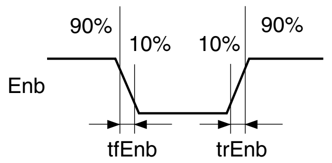
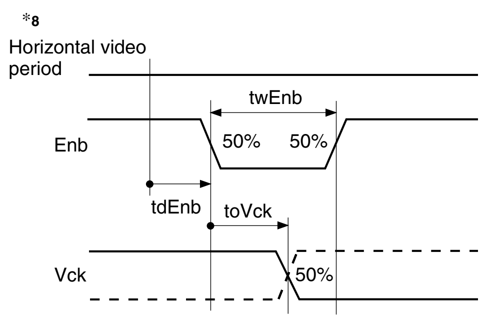
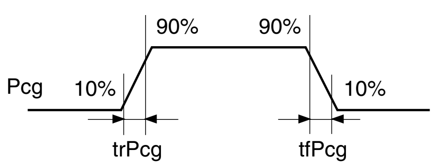
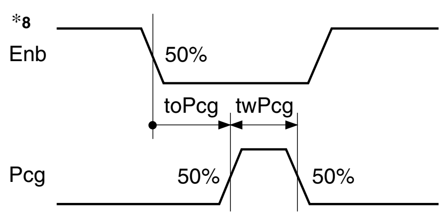
<Horizontal Shift Register Driving Waveform>

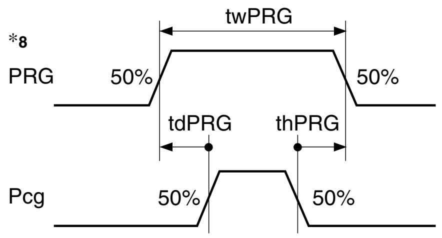
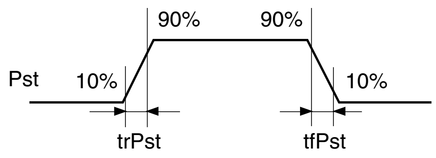
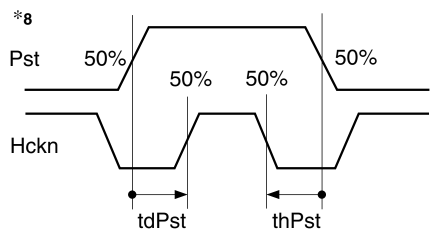
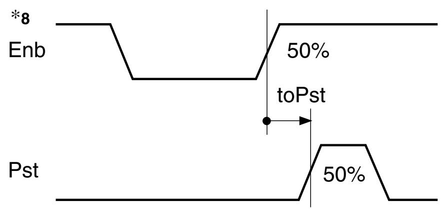
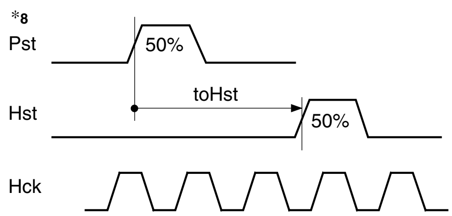
<table>
<tr><th colspan="2">Item</th><th>Symbol</th><th>Waveform</th><th>Conditions</th></tr>
<tr><td rowspan="4">HST</td><td>Hst rise time</td><td>trHst</td><td rowspan="2">
</td><td rowspan="2">• Hckn*5
duty cycle 50%
toHck = 0ns</td></tr>
<tr><td>Hst fall time</td><td>tfHst</td></tr>
<tr><td>Hst data
setup time</td><td>tdHst</td><td rowspan="2">
</td><td rowspan="2">• Hckn*5
duty cycle 50%
toHck = 0ns</td></tr>
<tr><td>Hst data
hold time</td><td>thHst</td></tr>
<tr><td rowspan="4">HCK</td><td>Hckn rise time*5</td><td>trHckn</td><td rowspan="2">
</td><td rowspan="2">• Hckn*5
duty cycle 50%
toHck = 0ns</td></tr>
<tr><td>Hckn fall time*5</td><td>tfHckn</td></tr>
<tr><td>Hck fall to
HckX rise time</td><td>toHck</td><td rowspan="2">
</td><td rowspan="2"></td></tr>
<tr><td>Hck rise to
HckX fall time</td><td>toHckX</td></tr>
<tr><td rowspan="6">DCK</td><td>Dckn rise time*6</td><td>trDckn</td><td rowspan="2">
</td><td rowspan="2">toDck1 = 0ns
toDck1X = 0ns
toDck2 = 0ns
toDck2X = 0ns</td></tr>
<tr><td>Dckn fall time*6</td><td>tfDckn</td></tr>
<tr><td>Dck1 rise to
Hck rise time</td><td>trDck1</td><td rowspan="2">
</td><td rowspan="2">toDck1 = 0ns
toDck1X = 0ns</td></tr>
<tr><td>Dck1 fall to
Hck fall time</td><td>tfDck1</td></tr>
<tr><td>Dck1 rise to
Dck1X fall time</td><td>toDck1X</td><td rowspan="2">
</td><td rowspan="2">trDck1 = 0ns</td></tr>
<tr><td>Dck1 fall to
Dck1X rise time</td><td>toDck1</td></tr>
</table>

*8 **Definitions:**
The right-pointing arrow (•→) means +.
The left-pointing arrow (←•) means –.
The black dot at an arrow (•) indicates the start of measurement.

Item		Symbol	Waveform	Conditions
DCK	Dck2 rise to HckX rise time	trDck2		toDck2 = 0ns toDck2X = 0ns
	Dck2 fall to HckX fall time	tfDck2		
	Dck2 rise to Dck2X fall time	toDck2X		trDck2 = 0ns
	Dck2 fall to Dck2X rise time	toDck2		

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data setup time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Horizontal video period completed to Enb fall time	tdEnb		
	Enb fall to Vck rise/fall time	toVck		
	Enb pulse width	twEnb		
PCG	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Enb fall to Pcg rise time	toPcg		
	Pcg pulse width	twPcg		

Item		Symbol	Waveform	Conditions
PRG	Pcg rise to PRG rise time	tdPRG		
	Pcg fall to PRG fall time	thPRG		
	PRG pulse width	twPRG		
PST	Pst rise time	trPst		
	Pst fall time	tfPst		
	Pst data setup time	tdPst		
	Pst data hold time	thPst		
	Enb rise to Pst rise time	toPst		
	Pst rise to Hst rise time	toHst		

Electrical Characteristics (Ta = 25°C, HV_{DD} = 15.5V, $VV_{DD}L$ = 15.5V, $VV_{DD}R$ = 15.5V, PV_{DD} = 15.5V, $VV_{DD}H$ = 15.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pin capacitance	HCKn	CHckn	—	15	20	pF	
	DCKn	CDckn	—	15	20	pF	
	HST	CHst	—	10	15	μA	
Input pin current	HCK		–1000	–500	—	μA	HCK = GND
	HCKX		–1000	–500	—	μA	HCKX = GND
	DCK1		–1000	–500	—	μA	DCK1 = GND
	DCK1X		–1000	–500	—	μA	DCK1X = GND
	DCK2		–1000	–500	—	μA	DCK2 = GND
	DCK2X		–1000	–500	—	μA	DCK2X = GND
	HST		–500	–200	—	μA	HST = GND
	RGT		–200	–100	—	μA	RGT = GND
Video signal input pin capacitance		Csig	—	210	250	pF	
Current consumption		IH	—	29	40	mA	HCKn, DCKn (3.33MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Conditions
Input pin capacitance	VCKL, VCKR	CVck	—	15	20	pF	
	VST	CVst	—	15	20	pF	
Input pin current	VCKL, VCKR, PCG		–500	–250	—	μA	VCKL,VCKR, PCG = GND
	VST, DWN, ENBL, ENBR		–150	–50	—	μA	VST, ENBL, ENBR, DWN = GND
Current consumption		IV	—	35	50	mA	VCK: (38.2kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel	PWR	—	800	900	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance	Rpin	0.4	1	—	MΩ

5. Uniformity improvement signal

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance for uniformity improvement signal	CPSIGo	—	1.0	1.5	nF

Electro-optical Characteristics (UXGA mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR	1	300	400	—	—
Optical transmittance		25°C	T	2	24	27	—	%
V-T characteristics	V_{90}	25°C	RV_{90-25}	3	0.67	0.81	0.93	V
			GV_{90-25}		0.78	0.88	0.95	
			BV_{90-25}		0.92	1.06	1.20	
		60°C	RV_{90-60}		0.76	0.91	1.04	
			GV_{90-60}		0.83	0.98	1.12	
			BV_{90-60}		0.97	1.11	1.24	
	V_{50}	25°C	RV_{50-25}		1.07	1.20	1.33	
			GV_{50-25}		1.15	1.28	1.51	
			BV_{50-25}		1.24	1.38	1.51	
		60°C	RV_{50-60}		1.19	1.33	1.46	
			GV_{50-60}		1.25	1.39	1.51	
			BV_{50-60}		1.33	1.46	1.60	
	V_{10}	25°C	RV_{10-25}		1.54	1.68	1.80	
			GV_{10-25}		1.60	1.75	1.88	
			BV_{10-25}		1.68	1.82	1.96	
		60°C	RV_{10-60}		1.69	1.83	1.97	
			GV_{10-60}		1.74	1.89	2.02	
			BV_{10-60}		1.81	1.96	2.10	
Response time	ON time	0°C	ton0	4	—	24.0	80.0	ms
		25°C	ton25		—	9.0	40.0	
	OFF time	0°C	toff0		—	99.0	200.0	
		25°C	toff25		—	27.0	70.0	
Flicker		60°C	F	5	—	–93.2	–40.0	dB
Image retention time		25°C	YT60	6	—	0	—	s
Cross talk		25°C	CTK	7	—	—	5	%

Anti-reflective Processing

When a retardation film which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a retardation film with anti-reflective processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage
HV_{DD} = 15.5V, $VV_{DD}L$, R = 15.5V, PV_{DD} = 15.5V
VVC = 7.5V, Vcom = 6.9V

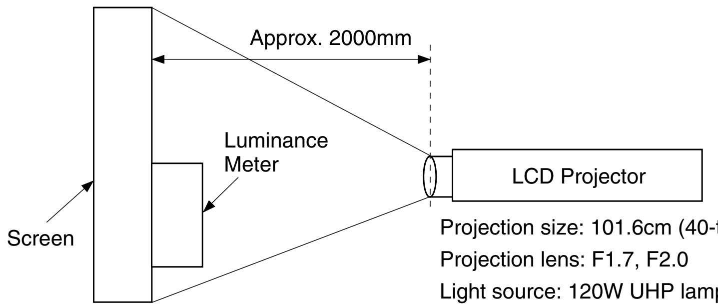
(2) Measurement temperature
25°C unless otherwise specified.

(3) Measurement point
One point in the center of the screen unless otherwise specified.

(4) Measurement systems
Two types of measurement systems are used as shown below.

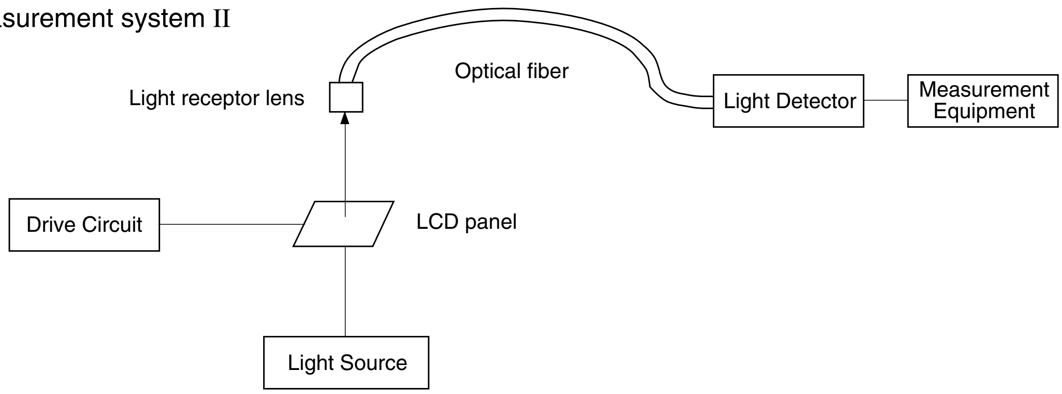
(5) Video input signal voltage (Vsig)
Vsig = 7.5 ± V_{AC} [V] (V_{AC} = signal amplitude)

* Measurement system I



Projection size: 101.6cm (40-type)
Projection lens: F1.7, F2.0
Light source: 120W UHP lamp, 120W × 4 UHP lamp
Incident lighting system: F#2.5
Polarizer: Side of incident light: Polatechno (SHC-A3U: Green)
Side of output light: Polatechno (SHC-A3U: Green)

* Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula.

$$CR = \frac{L\ (White)}{L\ (Black)}$$

L (White): Surface luminance of the center of the screen at the input signal amplitude V_{AC} = 0.5V.
L (Black): Surface luminance of the center of the screen at V_{AC} = 4.5V.
Both luminosities are measured by Measurement system I.

2. Optical Transmittance

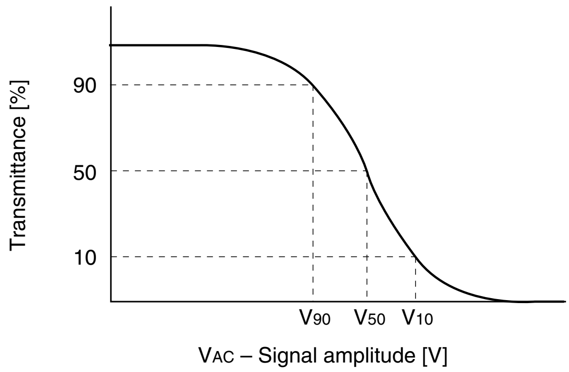
Optical Transmittance (T) is given by the following formula.

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100\ [\%]$$

"White luminance" means the maximum luminance on the screen at the input signal amplitude V_{AC} = 0.5V on Measurement system I.

3. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panel, are measured by Measurement system II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



4. Response Time

Response times ton and toff are defined by the following formulas respectively.

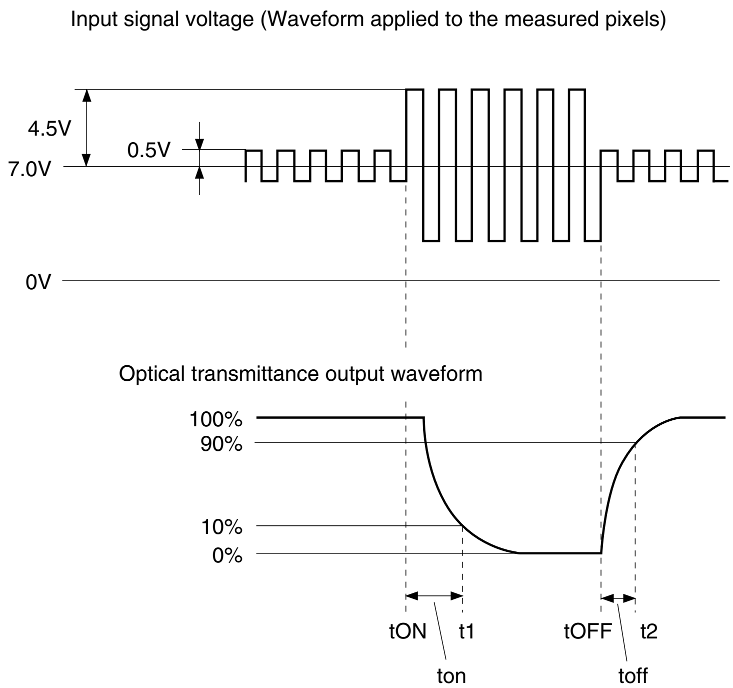
ton = t1 – tON

toff = t2 – tOFF

t1: time which gives 10% transmittance of the panel.

t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



5. Flicker

Flicker (F) is given by the following formula. DC and AC (UXGA: 30Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in Measurement system II.

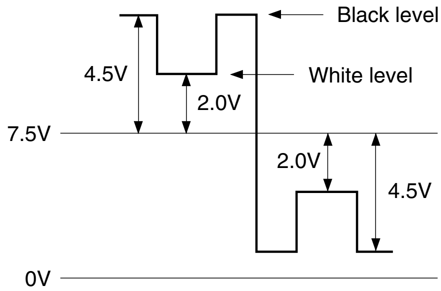
$$F\ [dB] = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\}$$

* Each input signal voltage for gray raster mode is given by Vsig = 7.5 ±V_{50} [V]
where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6. Image Retention Time

Apply the monoscope signal* to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 7.5 ± V_{AC} (V_{AC}: 3 to 4V). Judging by sight at the V_{AC} that holds the maximum image retention, measure the time till the residual image becomes indistinct.

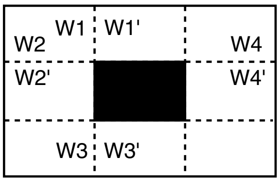
* Monoscope signal conditions
Vsig = 7.5 ± 4.5 or ± 2.0 [V]
(shown in the right figure)
Vcom = 6.9V



Vsig waveform

7. Cross Talk

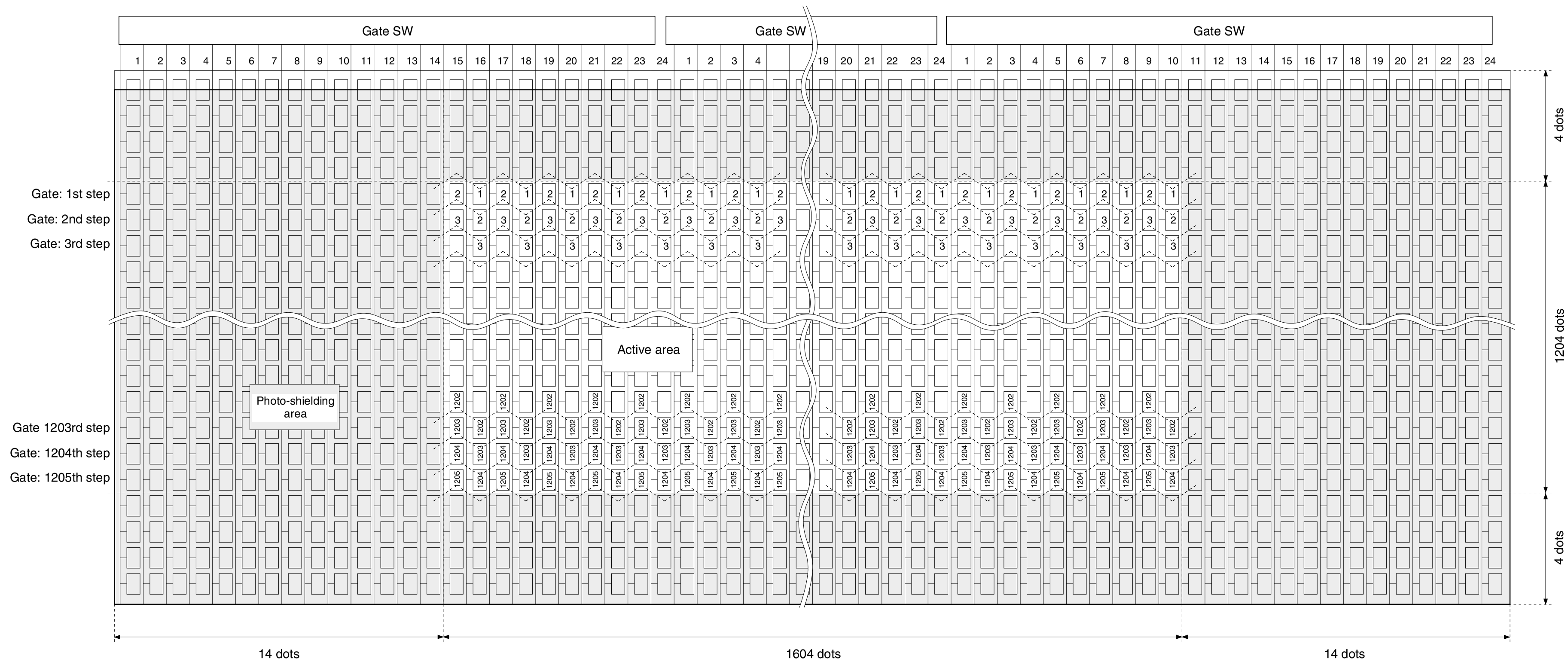
Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around a black window (Vsig = 4.5V/1V).



$$\text{Cross talk value CTK} = \left|\frac{Wi' - Wi}{Wi}\right| \times 100\ [\%]$$

1. Dot Arrangement

The dots are arranged in stripes. The shaded area is used for the dark border around the display.
(Viewed from the opposing side to the TFT substrate side)



1 : Pixel transistors turn on and off at the 1st gate step
2 : Pixel transistors turn on and off at the 2nd gate step
1205 : Pixel transistors turn on and off at the 1205th gate step

<Signal input>
Down scan: Input the previous line signals from VSIG2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22 and 24 to VSIG1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21 and 23, respectively.
Up scan: Input the previous line signals from VSIG1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21 and 23 to VSIG2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22 and 24, respectively.

2. LCD Panel Operations

[Description of basic operations]

- The pixel arrangements for the same gate are as shown on the previous page in order to perform dot-line inverse drive.
  Therefore, the VSIG1 to VSIG24 input signals must be suited to the respective arrangements.

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 1204 gate line electrodes sequentially in a single horizontal scanning period.

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 1604 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs for one dot) turn on to apply a video signal to the dot. The same procedures lead to the entire 1204 × 1604 dots to display a picture in a single vertical scanning period.

The LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and up/down setting modes are shown below.

RGT	Mode
H	Right scan
L	Left scan

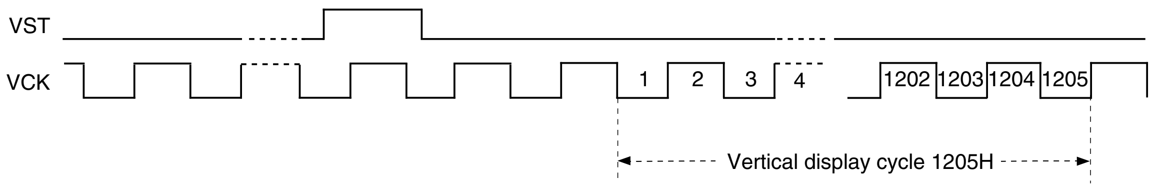
DWN	Mode
H	Down scan
L	Up scan

Right/left and up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

To locate the active area in the center of the panel in each mode, the start pulse, clock phase and polarity for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown below.

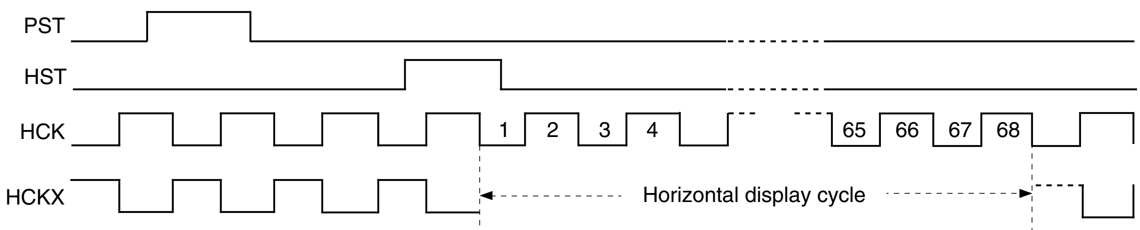
(1) Vertical direction display cycle (DWN = H, L)

(1.1) UXGA

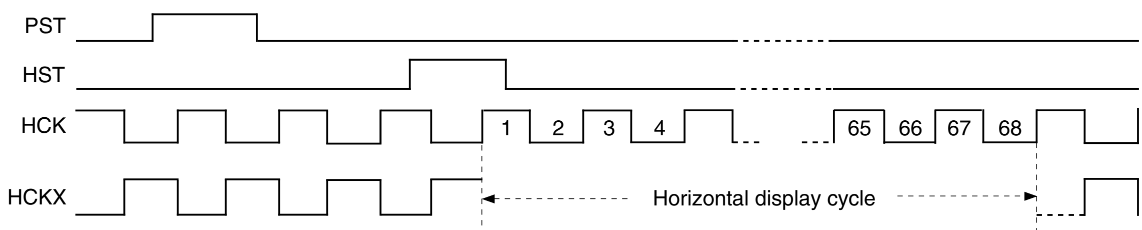


(2) Horizontal direction display cycle

(2.1) UXGA (RGT = H)



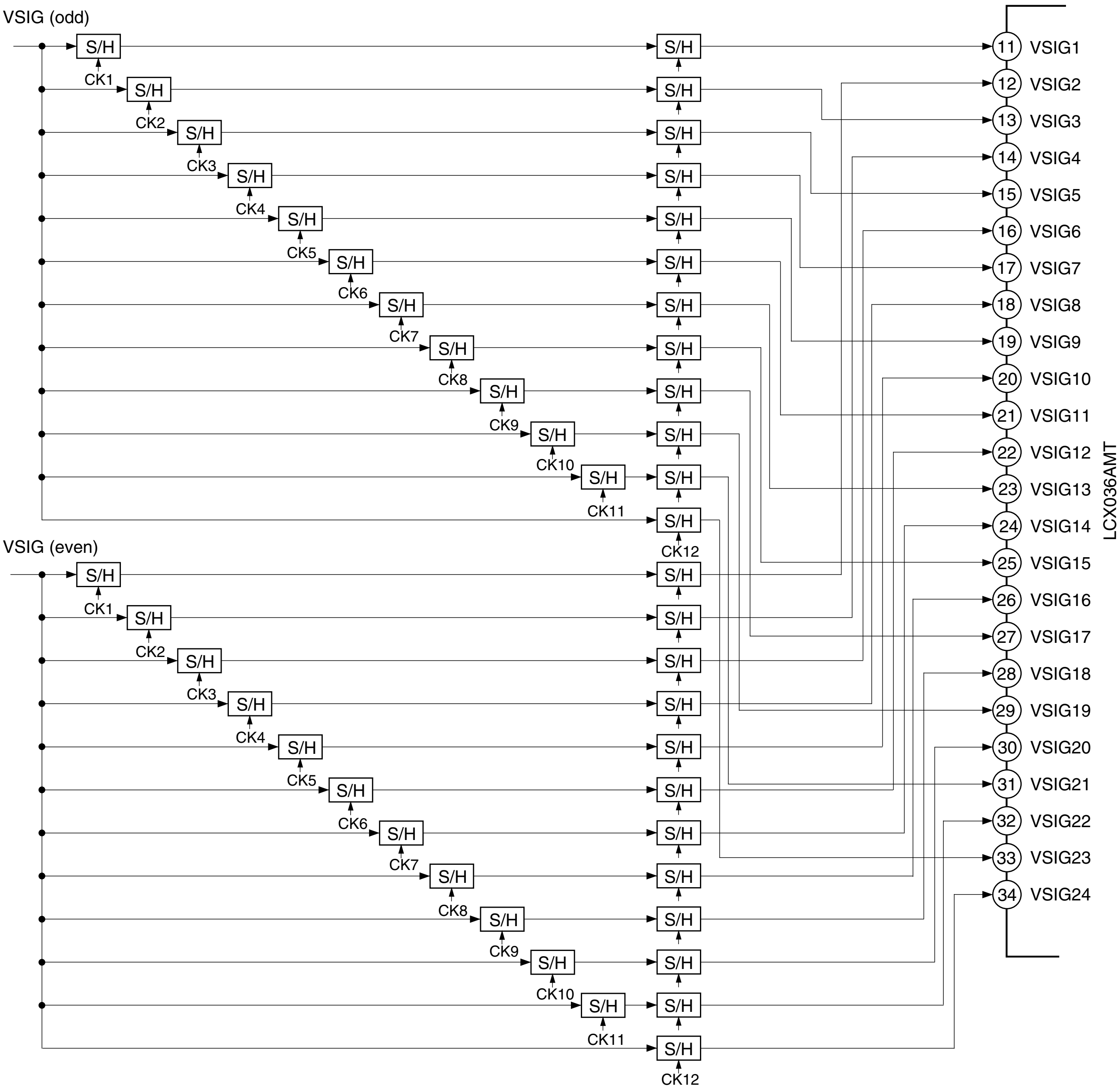
(2.2) UXGA (RGT = L)



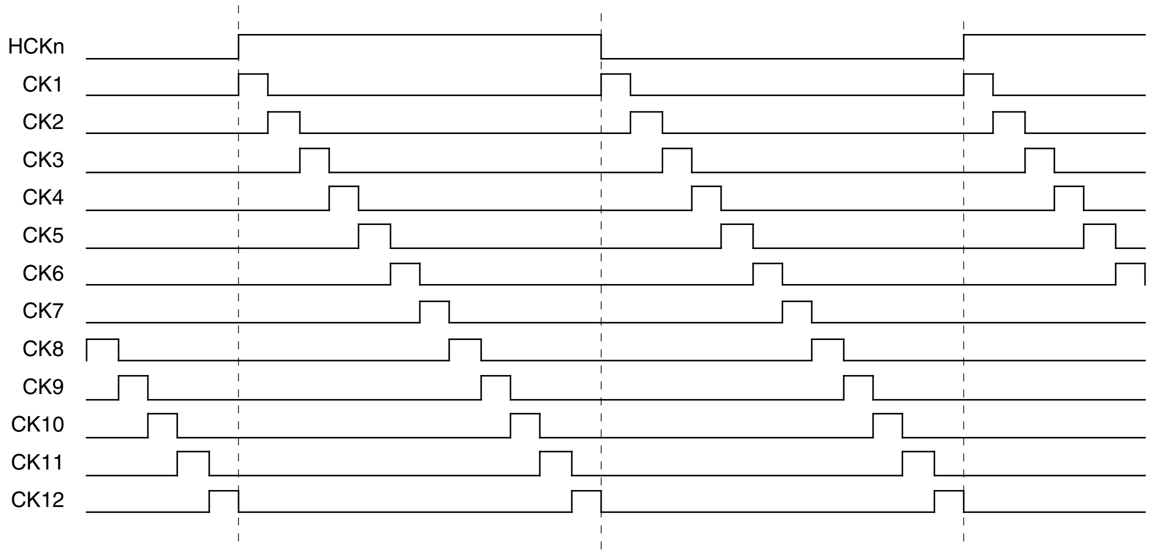
3. 24-dot Simultaneous Sampling

The horizontal shift register samples signals VSIG1 to VSIG24 simultaneously. This requires phase matching between signals VSIG1 to VSIG24 to prevent the horizontal resolution from deteriorating. Thus, phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High level). For left scan (RGT = Low level), the phase settings for signals VSIG1 to VSIG24 are exactly reversed.

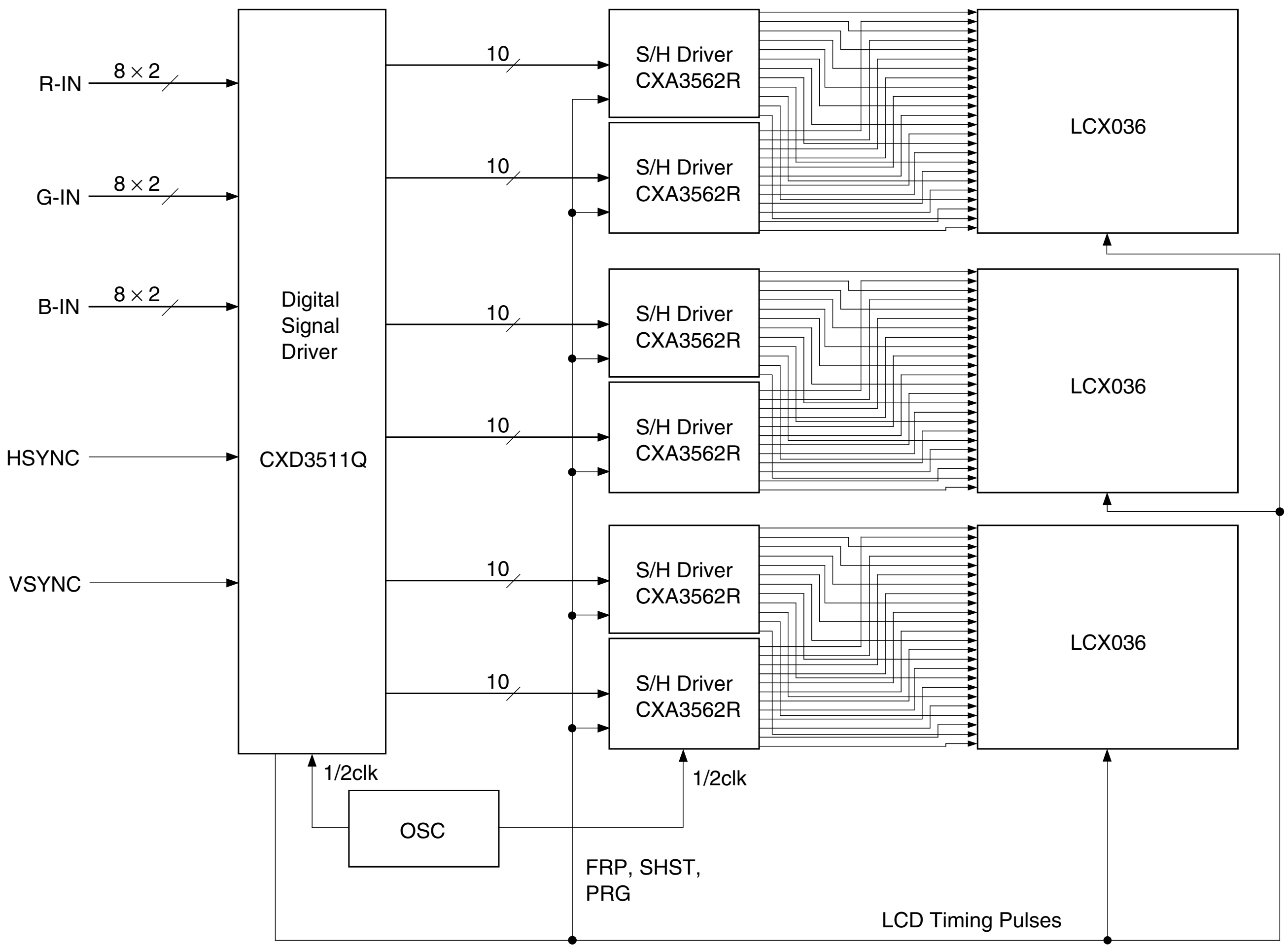


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



Notes on Handling

(1) Static charge prevention

Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.

a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

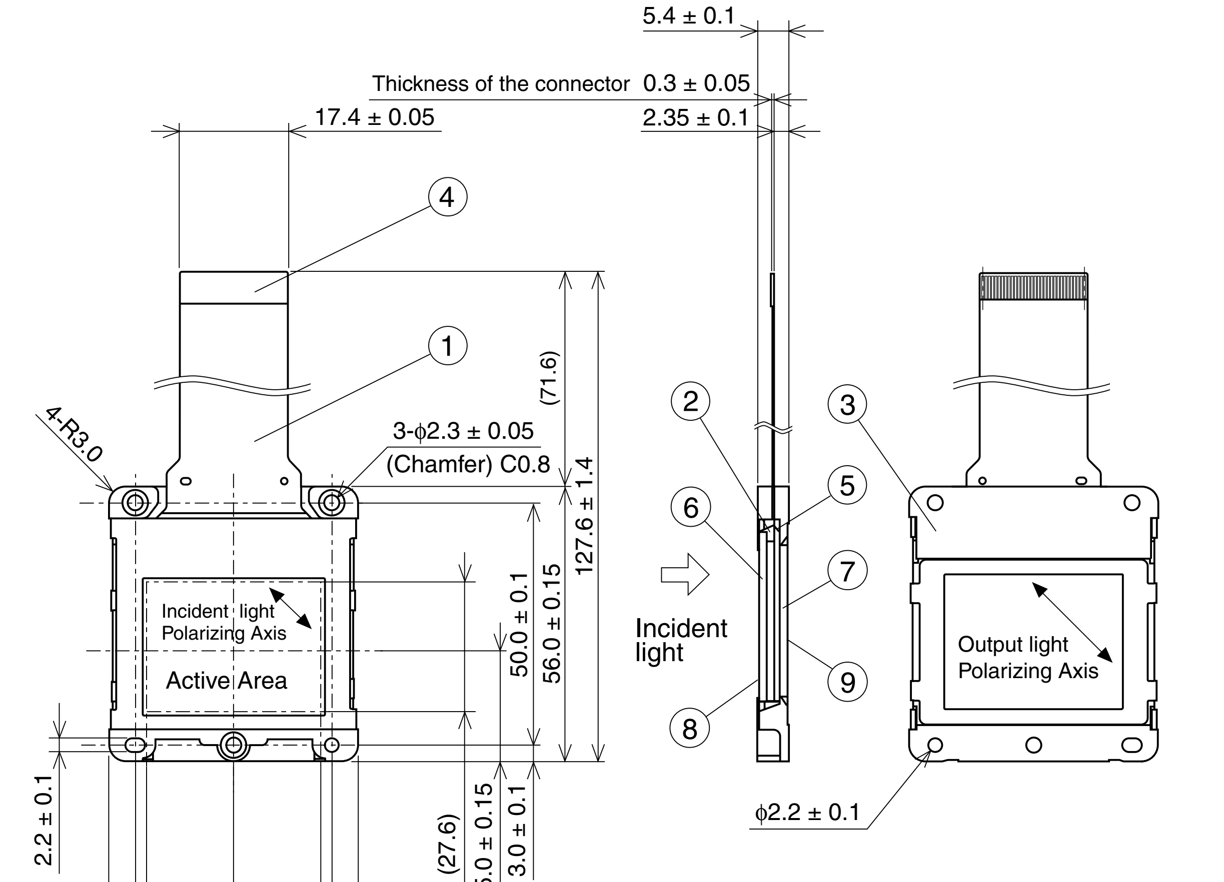
(2) Protection from dust and dirt

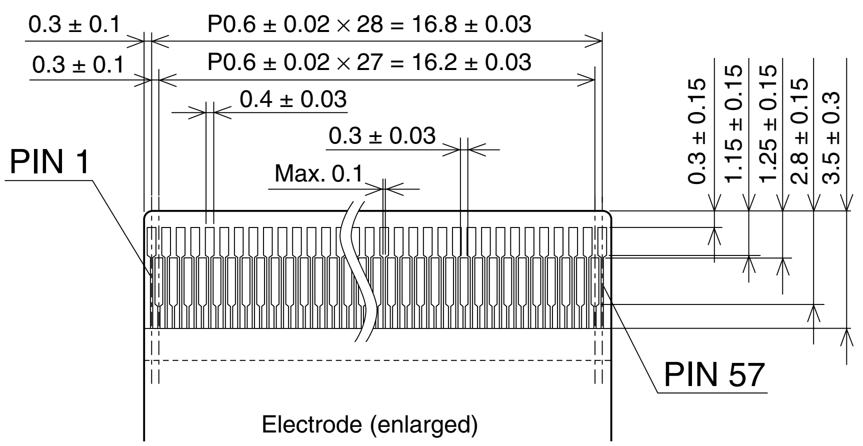
a) Operate in a clean environment.
b) When delivered, the panel surface (glass panel) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the glass panel.
c) Do not touch the glass panel surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
d) Use ionized air to blow dust off the glass panel.

(3) Other handling precautions

a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel.
c) Do not twist or bend the panel or panel frame.
d) Keep the panel away from heat sources.
e) Do not dampen the panel with water or other solvents.
f) Avoid storing or using the panel at a high temperature or high humidity, as this may result in panel damage.
g) The minimum radius of bending curvature for a flexible substrate is 1mm.
h) The torque required to tighten screws on a panel must be 3kg · cm or less.
i) Use an appropriate filter to protect the panel.
j) Do not apply pressure to portions (cover, etc.) other than the mounting hole.

Package Outline Unit: mm





The rotation angle of the active area relative to H and V is ± 1 .

No.	品名 Description
1	FPC
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Glass 1
7	Glass 2
8	Cover 1
9	Cover 2

Mass 25g